

**IN THE SPECIFICATION**

Please amend the specification as follows:

**The paragraph beginning at page 1, line 4 is amended as follows:**

**Cross Reference To Related Applications**

This application is related to the following co-pending, commonly assigned U.S. patent applications: "DRAM Cells with Repressed Memory Metal Oxide Tunnel Insulators," attorney docket no. 1303.019US1, ~~serial number~~ \_\_\_\_\_ serial number 09/945,395, "Flash Memory with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.014US1, ~~serial number~~ \_\_\_\_\_ serial number 09/945,507, "Dynamic Electrically Alterable Programmable Memory with Insulating Metal Oxide Interpoly Insulators," attorney docket no. 1303.024US1, ~~serial number~~ \_\_\_\_\_ serial number 09/945,498, and "Field Programmable Logic Arrays with Metal Oxide and/or Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.027US1, ~~serial number~~ \_\_\_\_\_ serial number 09/945,512, "SRAM Cells with Repressed Floating Gate Memory, Metal Oxide Tunnel Interpoly Insulators," attorney docket no. 1303.028US1, ~~serial number~~ \_\_\_\_\_ serial number 09/945,554, "Programmable Memory Address and Decode Devices with Low Tunnel Barrier Interpoly Insulators," attorney docket no. (~~Micron 01-0485~~) 1303.029US1, ~~serial number~~ \_\_\_\_\_ serial number 09/945,500, which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

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